A Novel Design of Spintronic Ternary Logic Circuits

Mohammad Sohorab Hossain

Abstract — This paper introduces novel ternary logic circuits using spintronic devices- magnetoresistive spin diodes and complementary magnetic junction (CMAT) logic architecture. Since ternary logic circuits can implement any function or compound logic using less gates and less circuit overhead such as interconnects and chip area than binary logic circuits, they are more energy efficient, compact, and good alternative to conventional binary logic circuits. And, since spintronics, being very fast, reliable, and compact, is a very good choice for beyond-CMOS logic design, we have designed spintronic ternary logic circuits to harness the benefits of spintronics and ternary logic system. We have demonstrated that proposed spintronic ternary basis circuit can perform ternary negation (NOT), conjunction (AND), disjunction (OR), and implication logic. The proposed ternary basis circuit is made of InAs/InMnAs magnetoresistive spin diode, InSb bilayer avalanche spin diode, and CMAT logic circuit. The CMAT logic circuit is built of several magnetic tunnel junctions (MTJ).

Index terms — Ternary logic, Spintronic, CMAT, Logic Circuit, Beyond-CMOS, Post-Neumann, Magnetoresistive device.

1 INTRODUCTION

Moore's law states that in every two year number of transistor in integrated circuit will be doubled. For last several decades the growth of semiconductor technology has somewhat followed Moore's law. But starting from around 2013 the growth has slowed down mainly due to the size of semiconductor devices (field effect transistor, FET) has nearly reached its physical limit. ICs beyond 5nm technology will drastically suffer from gate leakage current, increased process cost, increased power consumption, and decreased reliability [1-3]. Therefore, researchers all over the world are trying to find beyond-CMOS device that can be more efficient, lesser power consuming, reliable, and cost effective than CMOS ICs.

Historically computers are based on binary logic, but in 1958 Russian scientist made a ternary logic based computer SETUN [4-5]. Circuits used in SETUN were simplified using ternary logic architecture, and it required only 60% of the vacuum tube in a binary system [6-7]. This shows the immense possibility of ternary logic based devices as beyond-CMOS computing systems. However, since binary logic based CMOS devices have been kept pace with the demand until recently, only a handful of novel devices has been proposed to utilize ternary logic so far, such as, nanowire FETs, tunnel FETs, carbon nanotube (CNT) FETs, and grapheme FETs [8-14]. Besides device level implementation, there are several architecture level novelty also, such as, monolithic 3D architecture, multivalued logic architecture, and among many other neuromorphic architecture [15-20]. Despite of extensive research on these novel devices and architectures, none of them is free from disadvantages. Hence, none of them has been broadly accepted as post Neumann technology.

In this paper, we have introduced a spintronics based ternary logic circuit which can perform as fast, reliable, scalable, and cost effective beyond-CMOS device. Spintronics depend on spin of electron instead of charge. Though electron can have more than two spin states under magnetic field, in digital applications two states are significant- parallel and antiparallel spin. If the spin direction is in parallel with the imposed magnetic field, it is called parallel spin. And, if the spin direction is in antiparallel with the imposed magnetic field, it is called antiparallel spin. This properties of electron spin is used in Magnetic Tunnel Junction (MTJ) device. When two MTJs are arranged in pull-up and pull-down arrangement similar as CMOS structure, we get Complementary Magnetic Junction (CMAT) architecture [21]. In this paper, we used CMAT with two types of spin diodes- InAs/InMnAs magnetoresistive spin diode and InSb bilayer avalanche spin diode, to propose a new type of spintronic based ternary logic circuit.

2 Review Section

2.1 Ternary Logic

Three-valued logic or ternary logic can use two types of ternary systems- balanced ternary or unbalanced ternary. In balance and unbalanced ternary set of three values are {-1, 0, 1} and {0, 1, 2} respectively. In our work we will use balanced ternary system to build ternary logic circuits.

In their work, Arpasi et al. described ternary logic as a system L whose elements are valued in the set {0, 1, 2} (in our case the set is {-1, 0, 1}) and are called propositions or statements [22]. If A is a proposition, the value of A can be seen as a mapping v: L → {-1, 0, 1} such that,

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$$v(x) = \begin{cases} -1;\ if\ A\ is\ false \\ 0;\ if\ A\ is\ perhaps\ true, perhaps\ false, i.e., undefined \\ 1;\ if\ A\ is\ true \end{cases}$$

In ternary logic, following basic operations can be defined over L, [23];

- The negation ¬ (unary operation "not")
- The disjunction ∨ (binary operation "or")
- The conjunction ∧ (binary operation "and")
- The implication → (binary operation "if...then")

According to Arpasi et al. the system L is closed under any of these four operations, in the sense that if A, B ∈ L then ¬ A ∈ L, A ∨ B ∈ L, A ∧ B ∈ L, and A → B ∈ L. [22] So, if we can realize this four operations using spintronic circuits, we can essentially implement any complex function using ternary spintronic logic circuit.

The value of ¬ A, A ∨ B, A ∧ B, and A → B and other composed operations can be obtained by using the truth table shown in Table 1.

Table 1. Basic operations in the ternary logic

Sl. No.	A	B	Neg (A) $\neg A$	Conj (A,B) $A \wedge B$	Disj (A,B) $A \vee B$	Imp (A,B) $A \rightarrow B$
				min(A,B)	max(A,B)	
1	-1	-1	1	-1	-1	1
2	-1	0		-1	0	1
3	-1	1		-1	1	1
4	0	-1	0	-1	0	0
5	0	0		0	0	1
6	0	1		0	1	1
7	1	-1	-1	-1	1	-1
8	1	0		0	1	0
9	1	1		1	1	1

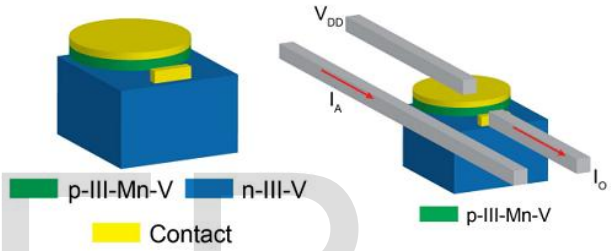
2.2 Magnetoresistive Spin diode

Magnetoresistive spin diode is one type of diode whose forward bias resistance can be controlled by magnetic field, and thus current through it can be controlled. [21] These spin diodes show two types of magnetoresistance, namely, positive and negative magnetoresistance.

i) Positively magnetoresistive spin diode:

This type of spin diode shows increased resistivity upon subjected to magnetic field. If there is no applied magnetic field, the spin diode acts as normal diode, i.e., if the applied voltage is above V_{bias} the diode acts in forward bias region and if the applied voltage is below V_{bias} the diode acts in reverse bias region. Now, in the forward bias condition if a magnetic field (above a threshold B_T) is applied at the p-n junction the resistance of the diode will increase and current through it will decrease.

In their work, Friedman et al. showed that InAs/InMnAs diode acts as a positively magnetoresistive spin diode [21]. Fig. 1.(a) shows the basic construction of a magnetoresistive spin diode. In Fig. 1.(b) an inverter is shown with a control wire placed near the p-n junction. An input control current I_A through the control wire creates a magnetic field which, in turn, regulates the resistance of the p-n junction and thus the output current I_O. If I_A is high, resulted magnetic field increases p-n junction resistance and suppresses the output current I_O. And, if I_A is low, resulted magnetic field decreases p-n junction resistance and increases the output current I_O. Hence, it can be seen that InAs/InMnAs spin diode shows positive magnetoresistance.



(a) (b)

Fig. 1. (a) InAs/InMnAs magnetoresistive spin diode. (b) Inverter. A control wire near the p-n junction carries input control current I_A which regulates the output current I_O. The positive terminal of the diode is connected to V_{DD} and the negative terminal is grounded. If I_A is high, resulted magnetic field decreases the output current [21].

ii) Negatively magnetoresistive spin diode:

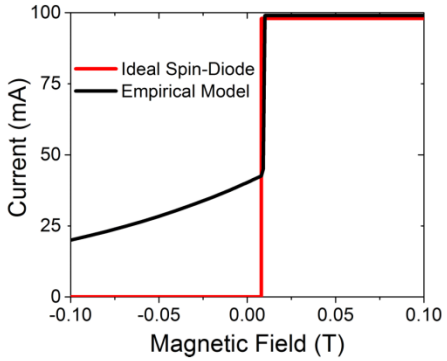


FIG. 2. I-B characteristics of negatively magnetoresistive spin diode. It shows almost ideal behavior, but has a finite "off" resistance and gradual switching [26].

This type of spin diode shows decreased resistivity upon subjected to magnetic field. If there is no applied magnetic field, the spin diode acts as normal diode, i.e., if the applied voltage is above V_{bias} the diode acts in forward bias region and if the

applied voltage is below V_{bias} the diode acts in reverse bias region. Now, in the forward bias condition if a magnetic field (above a threshold B_T) is applied at the p-n junction the resistance of the diode will decrease and current through it will increase.

In their work, Friedman et al. showed that InSb bilayer avalanche spin diode (in short, InSb avalanche spin diode) acts as a negative magnetoresistive spin diode [26]. Fig. 2 shows the I-B characteristics of this spin diode. InSb avalanche spin diode almost shows ideal switching behavior with a finite 'off' resistance and gradual switching [24]. Fig. 3 shows construction of an InSb avalanche spin diode. A bias voltage V_{DD} is applied to the drain contact and output current is taken from the source contact. Current I_A through the control wire creates a magnetic field which modulates the resistance of the p-n junction and thus the output current $I_{S\text{-}D}$. . If I_A is high, resulted magnetic field decreases p-n junction resistance and increases the output current $I_{S\text{-}D}$. And, if I_A is low, resulted magnetic field increases p-n junction resistance and suppresses the output current $I_{S\text{-}D}$. Hence, it can be seen that InSb avalanche spin diode shows negative magnetoresistance.

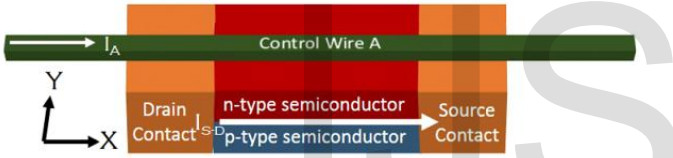


Fig. 3. InSb Bilayer avalanche spin-diode basis logic gate. Currents I_A creates a magnetic field across the semiconductor p-n junction that modulates Is−d [24].

So, from the above discussion it can be seen that, if a constant voltage above than forward bias voltage is applied across a magnetoresistive spin diode and a control current, i.e., control magnetic field is applied, two levels of output current emerges- a high current I_{High} and a low current I_{Low}. If we take I_{High} as logic '1' and I_{Low} as logic '0,' we can essentially build logic circuits [21] [24-26].

2.3 Magnetic tunnel Junction (MTJ)

Magnetic tunnel junction is a spintronic device based on the spin property of electron. If two ferromagnetic materials are separated by a non-magnetic insulator, we get a magnetic tunnel junction. In an MTJ electron from one ferromagnet can tunnel through the insulator to the second ferromagnet. Since, an electric current in a ferromagnet is composed of spin-up and spin-down electrons, and electron spin is conserved in tunneling process, if the magnetic moments of the two ferromagnets are in parallel more electrons will tunnel through the insulator. And, in case of antiparallel magnetic moments of the two ferromagnets less electron will tunnel through the insulator [27]. If the magnetization of the ferromagnets are M_1 and M_2 as shown in Fig. 4, the conductance of the MTJ is proportional to the cosine of the relative angle between M_1 and M_2, θ.

$$G(\theta) = \frac{1}{2}(G_P + G_{AP}) + \frac{1}{2}(G_P - G_{AP}).\cos\theta \quad -----(1)$$

where, G_{AP} and G_P are the conductance for θ = 180° (antiparallel state of two moments, AP) and θ = 0° (parallel state of two moments, P), respectively. The corresponding tunneling magnetoresistance (TMR) ratio is defined as:

$$TMR\ ratio = \frac{G_P - G_{AP}}{G_{AP}} = \frac{R_{AP} - R_P}{R_P} \quad -------(2)$$

where, R_{AP} and R_P are the resistances in the antiparallel and parallel state, respectively. The more the TMR ratio is, the more signal-to-noise ratio, i.e., reliability of the MTJ is.

2.4 Complimentary Magnetic Tunnel Junction Logic (CMAT logic)

In their work, Friedman et al. showed that two MTJ along with a control wire can be arranged in CMOS's pull-up pull-down structure to realize spintronic inverter and spintronic logic family [24-26]. They called this structure complimentary magnetic tunnel junction (CMAT) structure.

According to Friedman et al. MTJ with a control wire as shown in Fig. 5 is the building block of CMAT. It can be noted that among the two ferromagnets of the MTJ one ferromagnet requires stronger magnetic field than other to switch its magnetic polarization. Hence, it is called 'hard' ferromagnet. In this case, it is assumed that the magnetic polarization of the 'hard' ferromagnet is constant and in –z direction.

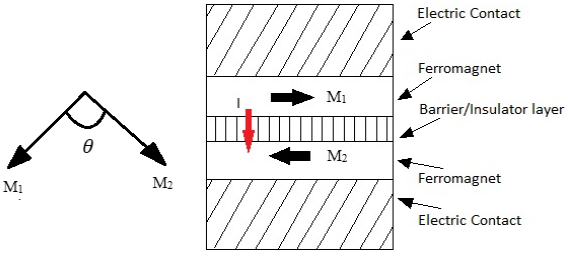


Fig. 4. Magnetizations M_1 and M_2 of the two ferromagnets in an MTJ. In this case, the magnetizations are in the film plane [27].

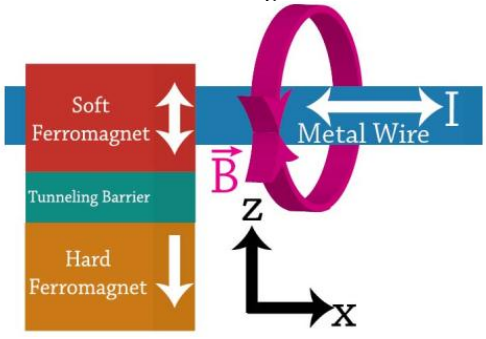


Fig. 5. MTJ with control wire. [26]

The magnetic polarization of the 'soft' ferromagnet can be switched by the magnetic field H produced by charge pulses in the control wire. Here H can be calculated using Ampere's law for a wire,

$$H = \frac{I}{2\pi r} \qquad ------ \quad (3)$$

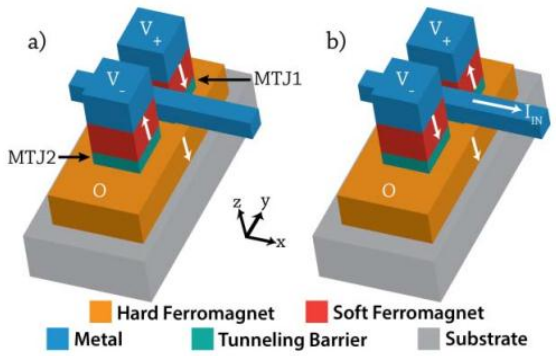


Fig. 6. CMAT inverter (a) before and (b) after a current I_{IN} is applied in the control wire [26].

The MTJ will be in its low resistance state if the "soft" ferromagnet is polarized in –z direction, i.e., parallel state of the two ferromagnets. It can be achieved by passing a charge pulse through the control wire in +x direction. If the charge pulse flows in –x direction, the "soft" ferromagnet will be polarized in +z direction resulting in antiparallel state of the two ferromagnets, which in turn will bring the MTJ to its high resistance state. Being non-volatile in nature, the ferromagnets maintain their magnetic polarization in the absence of external magnetic field [26].

According to Friedman et al. the inverter shown in Fig. 6 is the simplest CMAT logic gate. Assume, the "hard" ferromagnets constant polarization is in –z direction, and initially "soft" ferromagnets of MTJ1 and MTJ2 are polarized in –z and +z direction respectively. If an input control current I_{IN} is passed through the control wire in +x direction, the "soft" ferromagnets of MTJ1 and MTJ2 will be polarized in +z and -z direction respectively. So, MTJ1 will be in high resistance state and MTJ2 will be in low resistance state, which will result in an output voltage, $V_O = V_-$. Again, if the input control current I_{IN} through the control wire is in -x direction, the "soft" ferromagnets of MTJ1 and MTJ2 will be polarized in -z and +z direction respectively. So, MTJ1 will be in low resistance state and MTJ2 will be in high resistance state, which will result in an output voltage, $V_O = V_+$. Now, several inverters can be cascaded by using one inverter's output current as the input control current of another inverter [26].

In their work, Friedman et al. showed that a capacitor can be formed by inserting an insulating dielectric between the output node and the control wire that drives other logic gates. As a result, a charge pulse will be forced to flow toward (away from) the capacitor when the output node voltage switches low (high) [26].

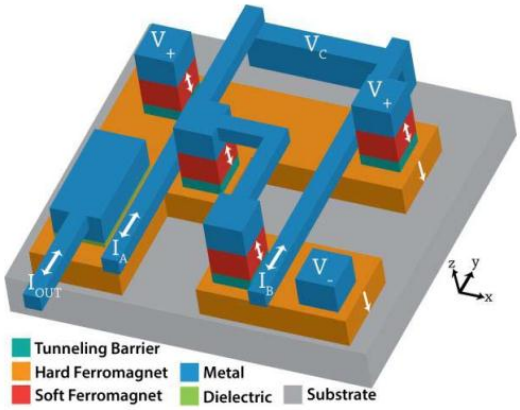


Fig. 7. CMAT basis AND/OR/NAND/NOR gate. [27]

Table 2. Positive directions of I_A, I_B, and I_{OUT} to realize AND, OR, NAND, and NOR gate using the CMAT basis circuit.

Operation	Positive direction of I_A	Positive direction of I_B	Positive direction of I_{OUT}
AND	+y	-y	+y
OR	-y	+y	-y
NAND	+y	-y	-y
NOR	-y	+y	+y

Friedman et al. used the CMAT basis circuit showed in Fig. 7 to realize binary AND/OR/NAND/NOR gate by taking input currents I_A, I_B and output current I_{OUT} being positive in either +y or –y direction [27]. For example, if we take positive directions of I_A, I_B, and I_{OUT} are in +y, -y, and +y directions respectively, the basis circuit acts as an AND gate (i.e., Output, O = A ∧ B). Table 2 shows the positive directions of I_A, I_B, and I_{OUT} to realize AND, OR, NAND, and NOR gate using the CMAT basis circuit.

3 Spintronic ternary logic circuits design

Let,

High current I_{High} (i.e., 100 mA) in any wire in +y or -y direction = 1 or -1, and

Absence of current (practically, I_{Low} = 30 mA in either +y or –y direction) = 0.

Before going into building ternary logic circuit, consider following two types of spin-diodes.

3.1 InSb avalanche spin diode

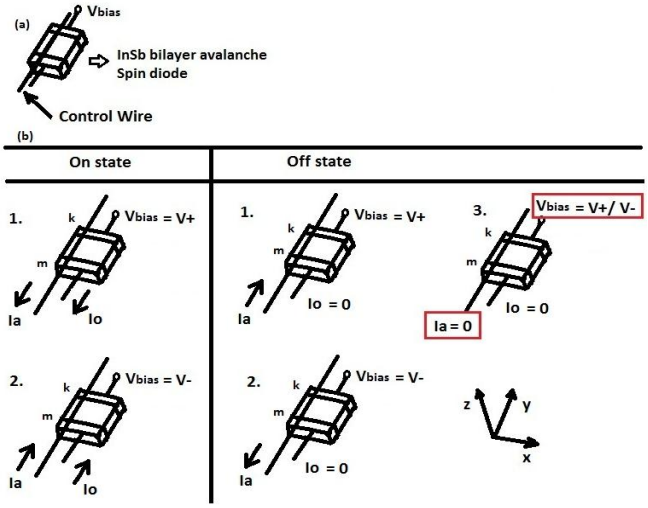


Fig. 8. InSb bilayer avalanche spin diode's, (a) symbol, and (b) On and Off states.

From Fig. 8. we can see that,

(1) If V_{bias} = V+ and current in the control wire I_a is in –y direction (i.e., from k to m), InSb spin diode will be in On state (i.e., $I_o \neq 0$).

(2) If V_{bias} = V- and I_a is in +y direction (i.e., from m to k), InSb spin diode will be in On state (i.e., $I_o \neq 0$).

(3) If V_{bias} = V+ and I_a is in +y direction (i.e., from m to k), InSb spin diode will be in Off state (i.e., $I_o = 0$).

(4) If V_{bias} = V- and I_a is in in –y direction (i.e., from k to m), InSb spin diode will be in Off state (i.e., $I_o = 0$).

(5) If I_a is 0 (i.e., = I_{Low}), irrespective of V_{bias} = V+ or V- InSb spin diode will be in Off state (i.e., $I_o = 0$).

Now, consider Fig. 9, where two InSb spin diodes are connected in parallel. Here control wires are routed in a way that, if $I_A \neq 0$ (as in 1, 2, 4, and 5 of Fig. 9), either one of the two InSb spin diodes will be in 'On' state and other one in 'Off' state (complementary relation between the spin diodes). So, there will be an output current, i.e., $I_o \neq 0$. For $I_A = 0$ (as in 3 and 6 of Fig. 9), $I_o = 0$ irrespective of V_{bias} = V+ or V- , since both #1 and #2 InSb spin diodes will be in Off state.

In all of these parallel connections, for one spin diode the control wire goes from point k to m, and for other spin diode it goes from point m to k. So, if the direction of control current causes one spin diode to be in 'Off' state, it will certainly make sure that other one is in 'On' state irrespective of V_{bias} = V+/V-.

3.2 InAs/InMnAs spin diode

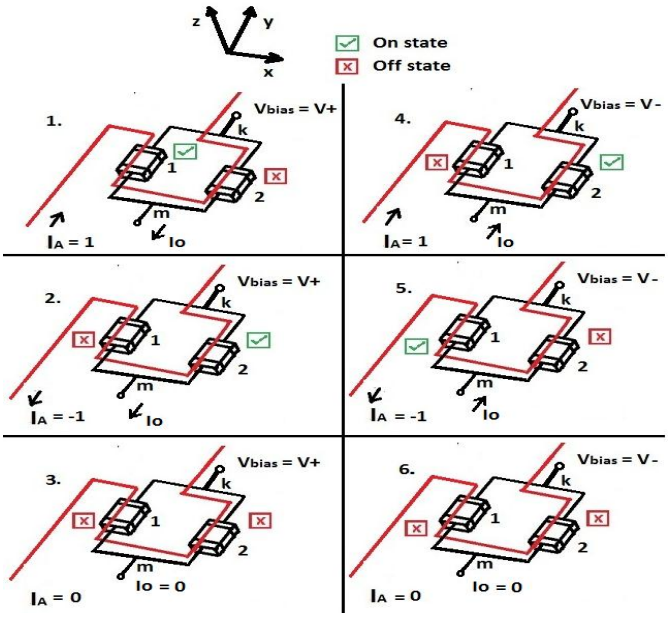


Fig. 9. Parallel connection of two InSb bilayer avalanche spin diodes. It can be seen that, if $I_A \neq 0$ (as in 1, 2, 4, and 5), either one of the two InSb spin diodes will be in On state, and output current, $I_o \neq 0$. For $I_A = 0$ (as in 3 and 6), $I_o = 0$.

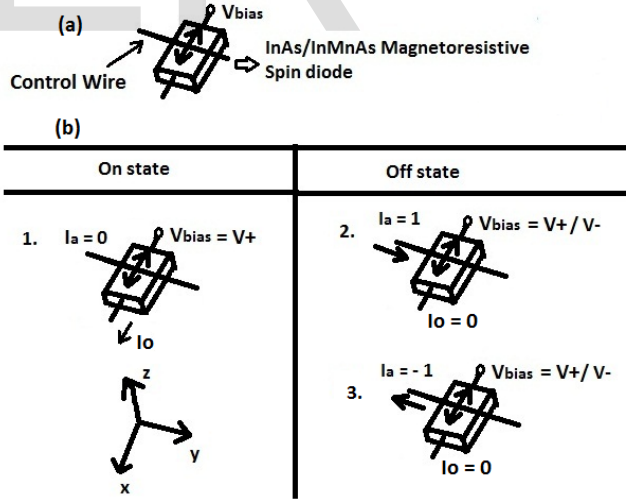


Fig. 10. InAs/InMnAs spin diode's, (a) symbol, (b) On and Off states. If control current $I_a = 0$, InAs/InMnAs spin diode will be in On state and $I_o \neq 0$. For $I_a = 1$ or -1, $I_o = 0$.

If control current $I_a = 0$ (as in 1 of Figure3), InAs/InMnAs spin diode will be in On state and $I_o \neq 0$. If $I_a = 1$ or -1 (as in 2 and 3 of Figure3), diode will be in Off state and $I_o = 0$.

Ternary logic circuit using CMAT logic is just an extension of binary CMAT logic circuit. Let's, first look at the ternary

inverter circuit, then we will see the ternary logic circuit for Ternary AND, OR, and Implication. (To make complete logic circuit in ternary logic, besides ternary 'AND' and 'OR' we will also need circuit for ternary Implication.)

3.3 Ternary Inverter

Table 3. Truth table for ternary inverter

Input, A	Direction of input Current, I_A	Neg (A) $\neg A$	Direction of output Current, I_o
-1	-y	1	-y
0		0	
1	+y	-1	+y

Here, input current, I_A (i.e., current in the control wire) has to be taken positive in +y direction, and output current, Io has to be taken positive in –y direction as shown in Fig. 11. Ternary inversion process is discussed below.

(i) When, I_A = -1 (Output has to be 1):

I_A is in –y direction. So, MJT 1 will be in parallel polarization with bottom hard ferromagnet (hereon similar case will be noted as, MJT 1 is in 'On' state). InSb diode #3 will have V_{bias} = V+ and control current in –y direction, so according to case 1 of Fig. 8 #3 will be in 'On' state. Therefore, voltage at #4 will be V+, and output current I_o in –y direction producing Output = 1 (since, I_o = 1 in –y direction).

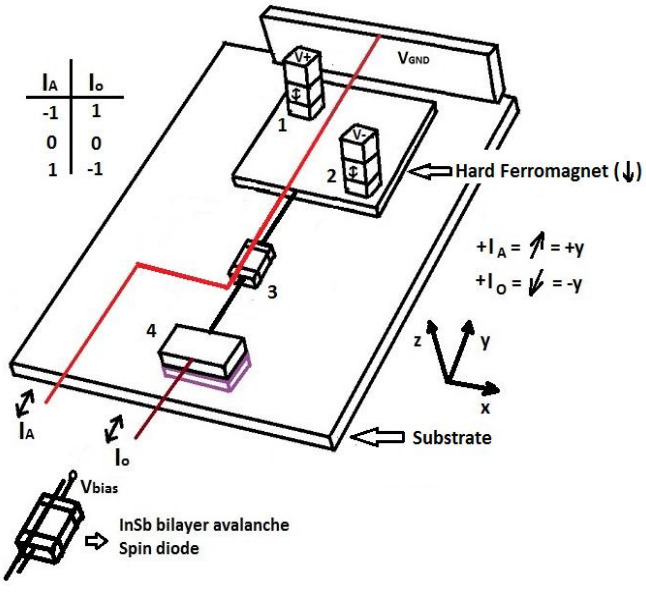


Fig. 11. CMAT logic implementation of Ternary Inverter.

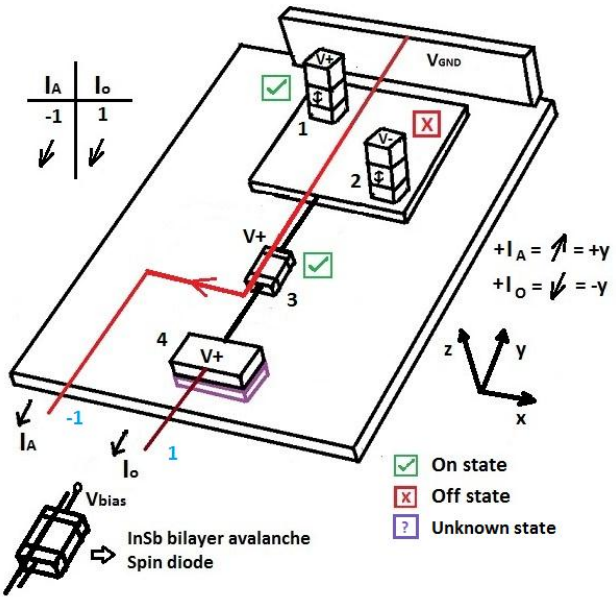


Fig. 12. Ternary Inverter with input, I_A = -1 and output, I_o = 1.

(ii) When I_A = 0 (Output has to be 0):

No input current means, there will be no control current for #3. Hence, according to case 5 of Fig. 8 #3 will be in 'Off' state. Consequently, voltage at #4 will be 0 and output current Io = 0 producing Output = 0.

[Practically it is possible that, there will be some output current due to leakage current (ILow) of #3, and its direction will be unknown. If previously MJT 1 was in 'On' state, this leakage current will be in –y direction. And, if previously MJT 2 was in 'On' state, this leakage current will be in +y direction.]

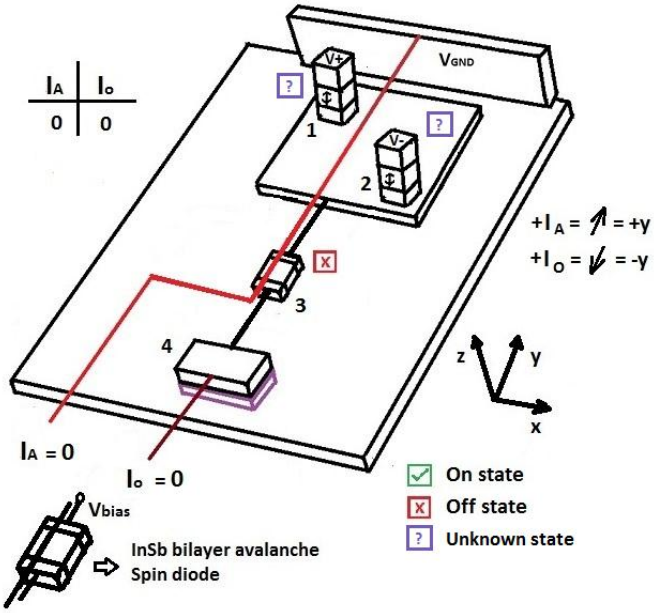


Fig. 13. Ternary Inverter with input, I_A = 0 and output, I_o = 0.

(iii) When $I_A = 1$ (Output has to be -1):

I_A is in +y direction. So, MJT 2 will be in 'On' state. InSb diode #3 will have V_{bias} = V- and control current in +y direction, so according to case 2 of Fig. 8 #3 will be in 'On' state. Therefore, voltage at #4 will be V-, and output current I_o in +y direction producing Output = -1 (since, I_o = -1 in +y direction).

3.4 Ternary logic circuit to implement ternary AND/OR/ Implication

We will first see the basic ternary logic circuit shown in Fig. 15 to implement ternary AND and OR. This basic circuit will be modified slightly by adding 2 more InAs/InMnAs spin diodes to implement ternary Implication function. This will be done because, unlike binary logic, in ternary logic Implication function can't be implemented using basic NOT, AND, and OR functions.

3.5 Basic ternary logic circuit

This basic circuit will be discussed in two parts.

(i) First part of basic ternary logic circuit:

This part is shown in Fig. 16. It is somewhat similar to the CMAT circuit to implement binary AND/OR/NAND/NOR mentioned in [27].

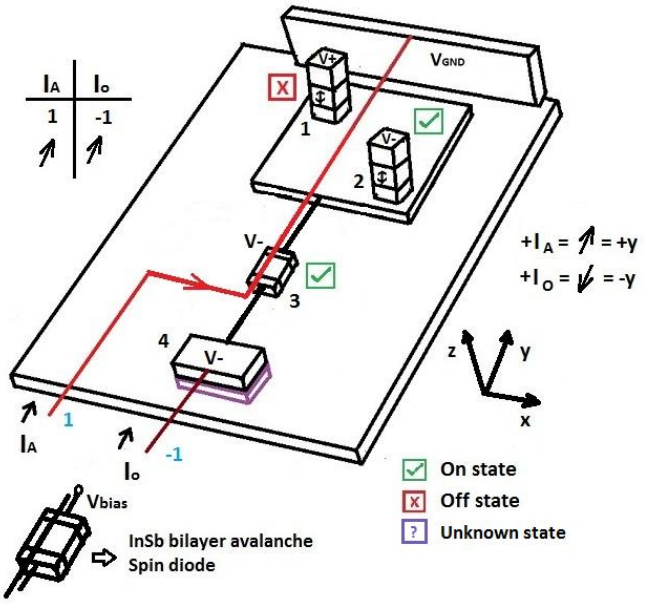


Fig. 14. Ternary Inverter with input, I_A = 1 and output, I_o = -1.

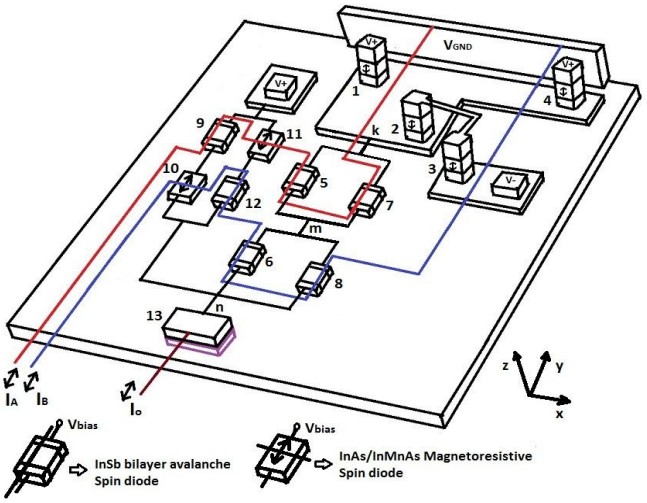


Fig. 15. Basic ternary logic circuit.

InSb spin diodes 5,7 and 6,8 are used here to ensure that for I_A = 0 and/or I_B = 0 there will be no direct/close path (case 5 of Fig. 9) between point k and n. This will cause first part of the basic circuit to be in 'Off' state and results in I_o = 0 (for I_A = 0 and/or I_B = 0) from this part. If $I_A \neq 0$ and $I_B \neq 0$, there will always be a direct/close path between point k and n, resulting $I_o \neq 0$. This will be called as 'On' state of the first part.

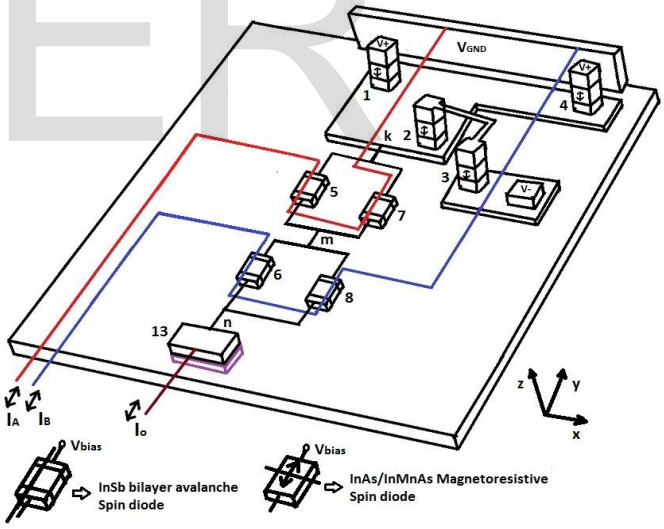


Fig. 16. First part of basic ternary logic circuit.

(ii) Second Part of basic ternary logic circuit:

In ternary logic, there are some input combinations where I_A = 0 and/or I_B = 0, but $I_o \neq 0$. In these cases, first part of the basic circuit will result in I_o = 0, so second part's job is to ensure that in these cases $I_o \neq 0$ by providing a direct path between V+ and point n as shown in Fig. 17.

If I_A is in –y direction and I_B = 0, #9 and #10 will be in 'On' state and I_o will be in –y direction. And, if I_A = 0 and I_B is in +y direction, #11 and #12 will be in 'On' state and I_o will be in –y direction. So, the second part will be in 'On' state for these two

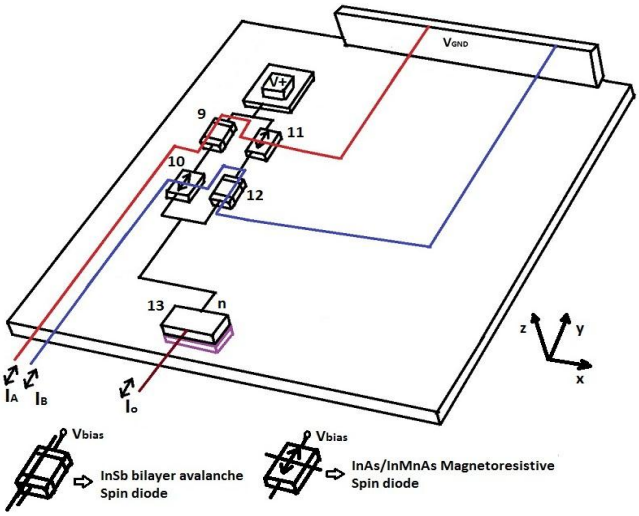


Fig. 17. Second part of basic ternary logic circuit.

input combinations and will always produce I_o in –y direction . This second part will be in 'Off' state for all other input combinations, and will result in $I_o = 0$ from this part.

3.6 Implementation of ternary AND logic

Table 4. Truth table for ternary AND

Sl. No.	A	B	Conj (A,B) $A \wedge B$		Currents	Positive direction, i.e., Logic '1'
1	-1	-1	-1		I_A	+y
2	-1	0	-1		I_B	-y
3	-1	1	-1		I_O	+y
4	0	-1	-1			
5	0	0	0			
6	0	1	0			
7	1	-1	-1			
8	1	0	0			
9	1	1	1			

If we take positive direction of I_A along +y axis, I_B along –y axis, and I_O along +y axis, basic ternary circuit in Fig. 15 will perform as ternary AND gate. It is shown in Fig. 18.

For input combination # 1, 3, 7, and 9 of AND logic shown in Table 4, none of the inputs is 0. So, for these combinations second part of the basic circuit will be in 'Off' state (as discussed in case (ii) of article 2.1), and we only have to discuss about the first part.

For input combination # 2, 4, 5, 6, and 8 of AND logic shown in Table 4, at least one of the inputs is 0. So, for these combinations first part of the basic circuit will be in 'Off' state (as discussed in case (i) of article 2.1), and we only have to discuss about the second part.

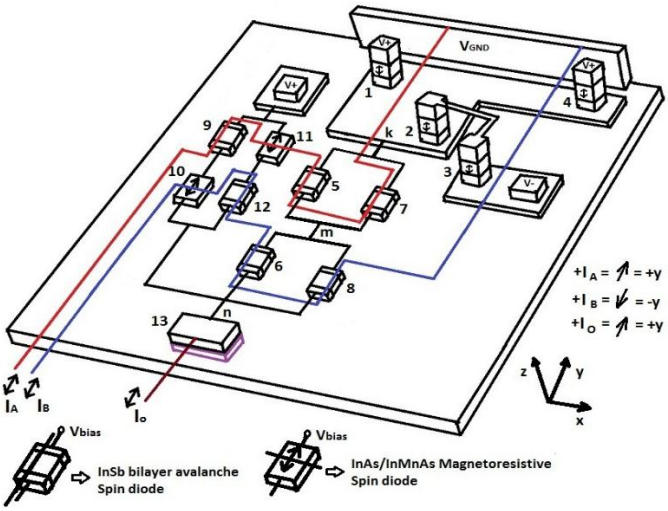


Fig. 18. Ternary basic circuit performing Ternary AND logic.

We will only include figures to demonstrate different input combinations.

(1) Input combination #1 ($I_A = -1$, $I_B = -1$, and $I_O = -1$):

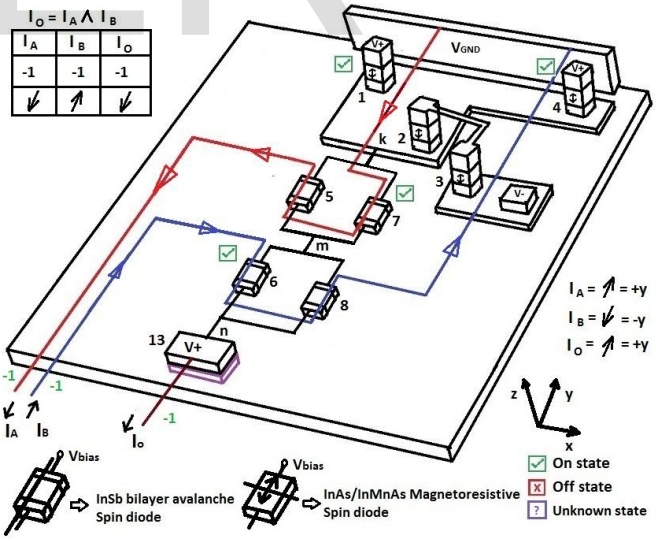


Fig. 19. Ternary AND logic, input combination #1. The voltage at point k is V+, and there is a close path from k to n through #7 and #6. So, voltage at n is V+ and output current $I_O = -1$.

(2) Input combination #3 ($I_A = -1$, $I_B = 1$, and $I_O = -1$):

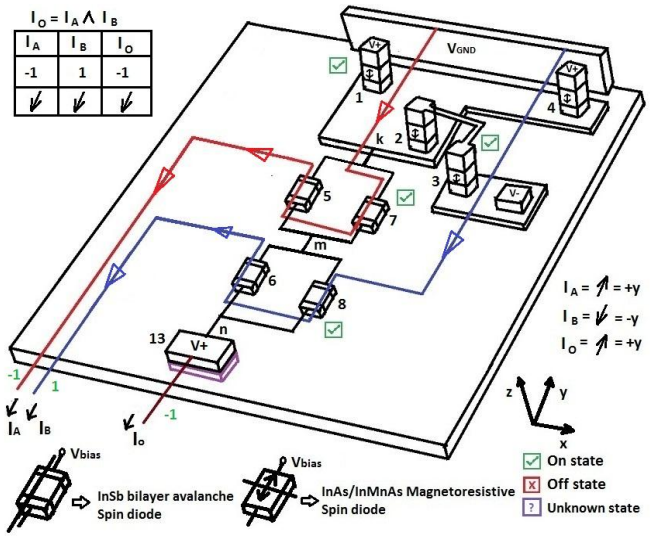


Fig. 20. Ternary AND logic, input combination #3. The voltage at point k is V+, and there is a close path from k to n through #7 and #8. So, voltage at n is V+ and output current $I_O = -1$.

(3) Input combination #7 ($I_A = 1$, $I_B = -1$, and $I_O = -1$):

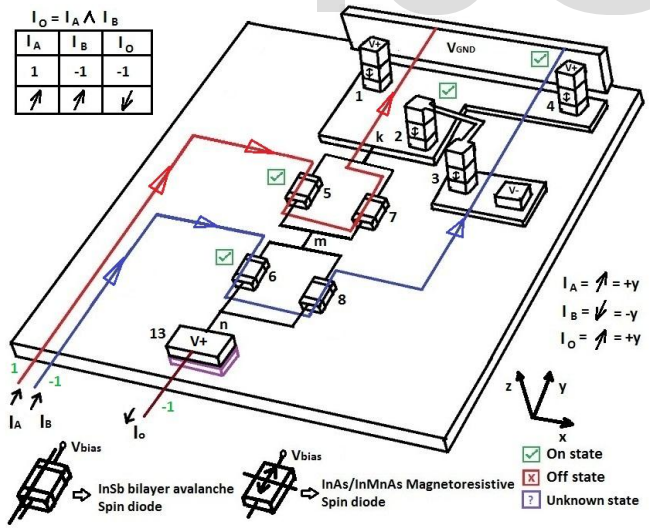


Fig. 21. Ternary AND logic, input combination #7. The voltage at point k is V+, and there is a close path from k to n through #5 and #6. So, voltage at n is V+ and output current $I_O = -1$.

(4) Input combination #9 ($I_A = 1$, $I_B = 1$, and $I_O = 1$):

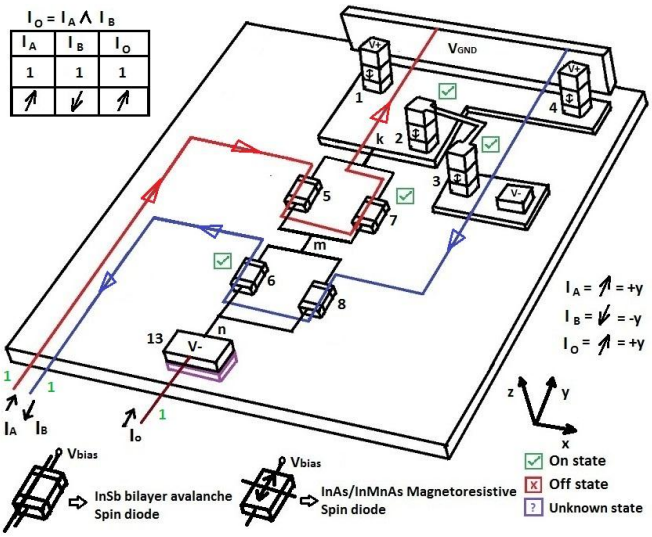


Fig. 22. Ternary AND logic, input combination #9. The voltage at point k is V-, and there is a close path from k to n through #7 and #6. So, voltage at n is V- and output current $I_O = 1$.

(5) Input combination #2 ($I_A = -1$, $I_B = 0$, and $I_O = -1$):

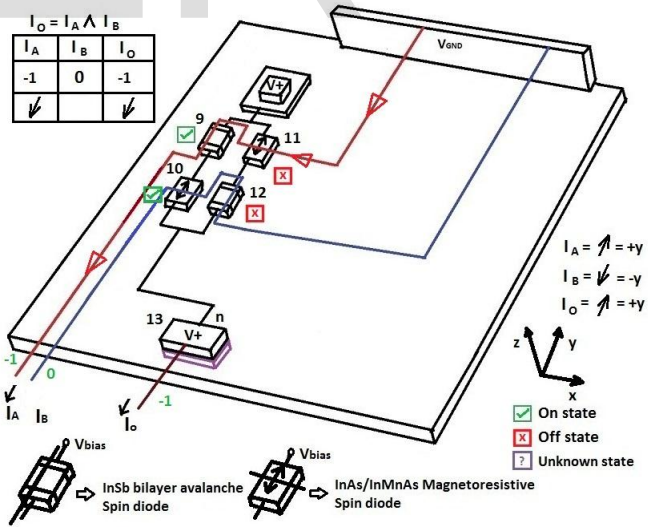


Fig. 23. Ternary AND logic, input combination #2. There is a closed path from source V+ to point n through #9 and #10. So, the voltage at point n is V+ and output current $I_O = -1$.

(6) Input combination #4 ($I_A = 0$, $I_B = -1$, and $I_O = -1$):

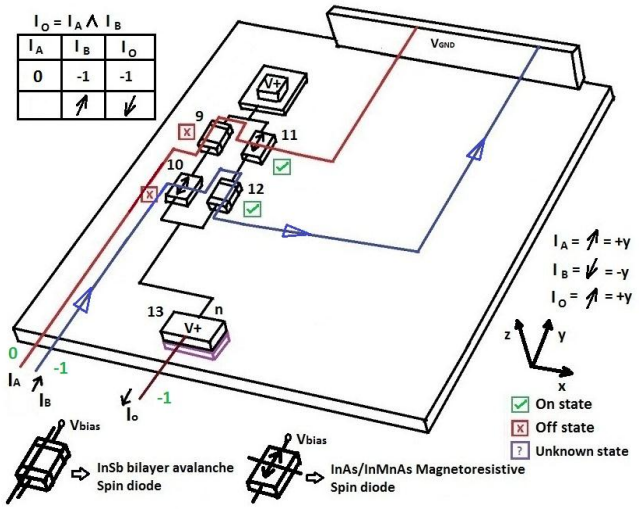


Fig. 24. Ternary AND logic, input combination #4. There is a closed path from source V+ to point n through #11 and #12. So, the voltage at point n is V+ and output current $I_O = -1$.

(7) Input combination #5 ($I_A = 0$, $I_B = 0$, and $I_O = 0$):

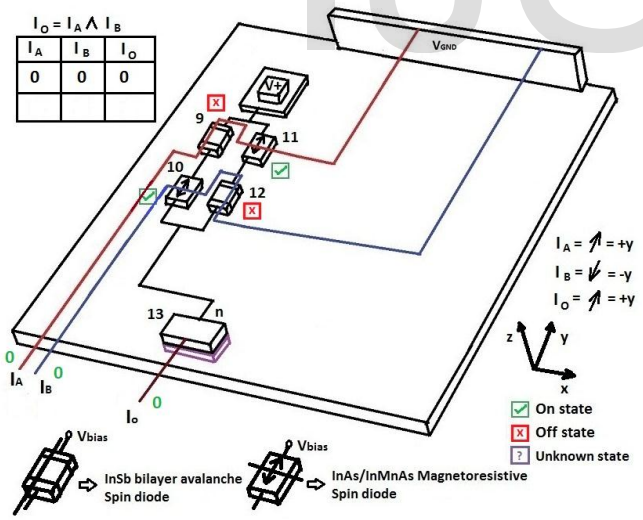


Fig. 25. Ternary AND logic, input combination #5. There is no closed path from source V+ to point n. So, there will be no output current, i.e., $I_O = 0$.

(8) Input combination #6 ($I_A = 0$, $I_B = 1$, and $I_O = 0$):

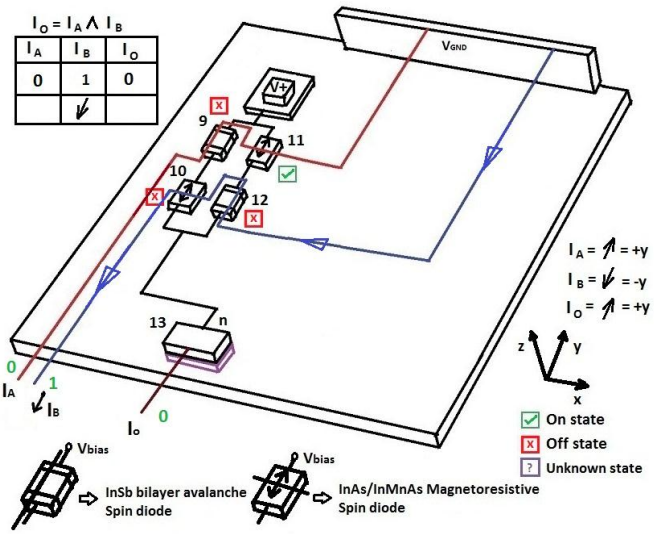


Fig. 26. Ternary AND logic, input combination #6. There is no closed path from source V+ to point n. So, there will be no output current, i.e., $I_O = 0$.

(9) Input combination #8 ($I_A = 1$, $I_B = 0$, and $I_O = 0$):

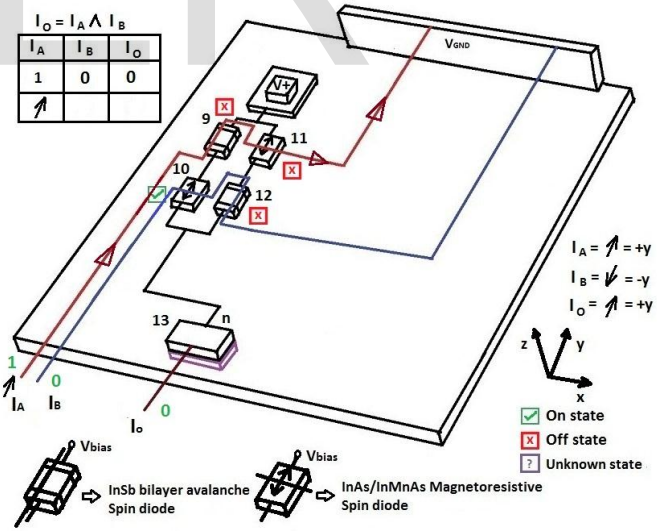


Fig. 27. Ternary AND logic, input combination #8. There is no closed path from source V+ to point n. So, there will be no output current, i.e., $I_O = 0$.

3.7 Implementation of ternary OR logic

Instead of showing all input combinations of OR logic using figures, we will show that by choosing positive directions of I_A, I_B, and I_O along different axes than ternary AND logic we can

implement ternary OR logic using same basic logic circuit shown in Fig. 15.

Table 5. Truth table to show that $A \vee B \Leftrightarrow \neg(\neg A \wedge \neg B)$.

Sl. No.	A	B	$\neg A$	$\neg B$	$A \vee B$	$\neg A \wedge \neg B$	$\neg(\neg A \wedge \neg B)$
1	-1	-1	1	1	-1	1	-1
2	-1	0	1	0	0	0	0
3	-1	1	1	-1	1	-1	1
4	0	-1	0	1	0	0	0
5	0	0	0	0	0	0	0
6	0	1	0	-1	1	-1	1
7	1	-1	-1	1	1	-1	1
8	1	0	-1	0	1	-1	1
9	1	1	-1	-1	1	-1	1

From the truth table we can see that,

$$A \vee B \Leftrightarrow \neg(\neg A \wedge \neg B).$$

Let,

$$C = A \vee B \Leftrightarrow \neg(\neg A \wedge \neg B). \quad ------(1)$$

$$P = Q \wedge R \quad ------(2)$$

Comparing equation (1) and (2) we get,

$$\neg A \equiv Q \quad \Rightarrow \quad A \equiv \neg Q$$

$$\neg B \equiv R \quad \Rightarrow \quad B \equiv \neg R$$

$$C \equiv \neg P$$

So, to implement OR logic using same basic circuit as AND logic we have to take,

$$\text{Positive direction of } I_{A(OR)} = -(\text{Positive direction of } I_{A(AND)}) = -(+y) = -y\ (\swarrow)$$

$$\text{Positive direction of } I_{B(OR)} = -(\text{Positive direction of } I_{B(AND)}) = -(-y) = +y\ (\nearrow)$$

$$\text{Positive direction of } I_{O(OR)} = -(\text{Positive direction of } I_{O(AND)}) = -(+y) = -y\ (\swarrow)$$

Actually, OR logic's working mechanism will follow AND logic's working mechanism in the following manner,

#1 of OR logic is equivalent to #9 of AND logic shown in Fig. 22.
#2 of OR logic is equivalent to #8 of AND logic shown in Fig. 27.
#3 of OR logic is equivalent to #7 of AND logic shown in Fig. 21.
#4 of OR logic is equivalent to #6of AND logic shown in Fig. 26.
#5 of OR logic is equivalent to #5 of AND logic shown in Fig. 25.
#6 of OR logic is equivalent to #4 of AND logic shown in Fig. 24.
#7 of OR logic is equivalent to #3 of AND logic shown in Fig. 20.
#8 of OR logic is equivalent to #2 of AND logic shown in Fig. 23.
#9 of OR logic is equivalent to #1 of AND logic shown in Fig. 19.

3.8 Implementation of ternary Implication logic

Instead of showing all input combinations of Implication logic using figures, we will show that by choosing positive directions of I_A, I_B, and I_O along different axes than ternary AND logic we can implement all but one input combinations (#1 to #9 except #5) of ternary Implication logic using same basic logic circuit shown in Fig. 15. Then, to implement that exception (input combination #5), we will add two serially connected InAs/InMnAs spin diodes in the second part of the basic circuit.

From table 6 we can see that $A \rightarrow B$ and $\neg(A \wedge \neg B)$ are same except for input combination #5. That is, for input combinations #1 to #4 and #6 to #9, $A \rightarrow B \Leftrightarrow \neg(A \wedge \neg B)$.

Table 6. Truth table to show that $A \rightarrow B \nLeftrightarrow \neg A \vee B$

Sl. No.	A	B	$\neg A$	$\neg A \vee B = \neg(A \wedge \neg B)$	Imp (A,B) $A \rightarrow B$
1	-1	-1	1	1	1
2	-1	0	1	1	1
3	-1	1	1	1	1
4	0	-1	0	0	0
5	**0**	**0**	**0**	**0**	**1**
6	0	1	0	1	1
7	1	-1	-1	-1	-1
8	1	0	-1	0	0
9	1	1	-1	1	1

Now consider,

$$C = A \rightarrow B \Leftrightarrow \neg(A \wedge \neg B) \quad ------(3)$$

$$P = Q \wedge R \quad ------(4)$$

Comparing equation (3) and (4) we get,

$$A \equiv Q$$

$$\neg B \equiv R \quad \Rightarrow \quad B \equiv \neg R$$

$$C \equiv \neg P$$

So, to implement Implication logic for input combinations #1 to #4 and #6 to #9 using same basic circuit as AND logic we have to take,

Positive direction of $I_{A(Imp)}$
$= $ (Positive direction of $I_{A(AND)}$) $= +y$ ($\nearrow$)

Positive direction of $I_{B(OR)}$
$= -$ (Positive direction of $I_{B(AND)}$)
$= -(-y) = +y$ ($\nearrow$)

Positive direction of $I_{O(OR)}$
$= -$ (Positive direction of $I_{O(AND)}$)
$= -(+y) = -y$ ($\swarrow$)

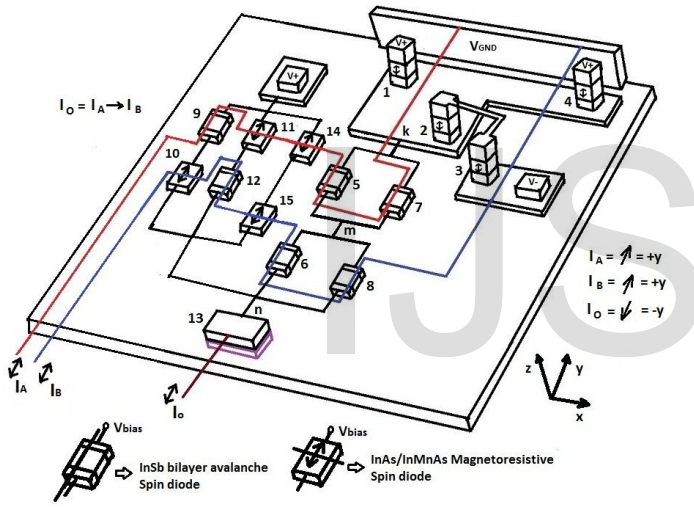


Fig. 28. Circuit to implement ternary Implication logic. Here, two InAs/InMnAs spin diodes #14 and #15 are added to basic ternary logic circuit. These two spin-diodes will be in 'ON' state when $I_A = 0$ and $I_B = 0$ (input combination #5) producing an output current $I_O = 1$.

Actually, Implication logic's working mechanism will follow AND logic's working mechanism in the following manner,

#1 of Implication logic is equivalent to #3 of AND logic shown in Fig. 20.
#2 of Implication logic is equivalent to #2 of AND logic shown in Fig. 23.
#3 of Implication logic is equivalent to #1 of AND logic shown in Fig. 19.
#4 of Implication logic is equivalent to #6of AND logic shown in Fig. 26.
#6 of Implication logic is equivalent to #4 of AND logic shown in Fig. 24.
#7 of Implication logic is equivalent to #9 of AND logic shown in Fig. 22.
#8 of Implication logic is equivalent to #8 of AND logic shown in Fig. 27.
#9 of Implication logic is equivalent to #7 of AND logic shown in Fig. 21.

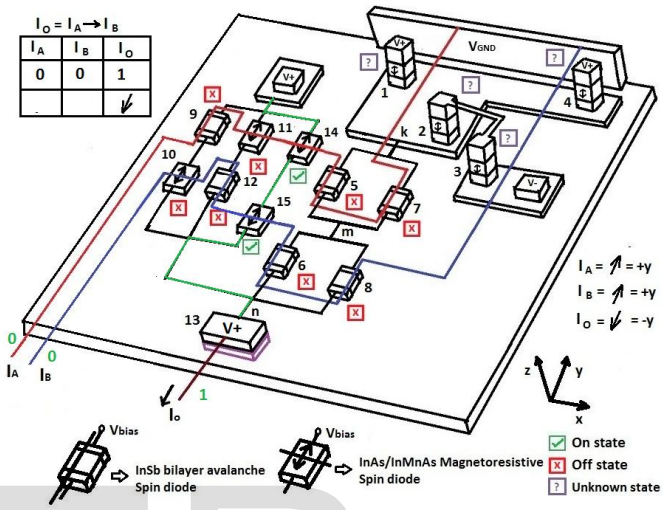


Fig. 29. Ternary Implication logic, input combination #5. There is a closed path (marked in green color) from source V+ to point n. So, there will be an output current, i.e., $I_O = 1$.

Modified circuit to implement input combination #5 of Implication logic is shown in Fig. 28. The modification is done only in the second part of the basic circuit and the added series connection of #14 and #15 will provide a close path from source V+ to point n only for input combination #5, i.e., when both $I_A = 0$ and $I_B = 0$. For all other combinations this added branch will be open, and this circuit will work as the basic circuit does.

Working of the ternary Implication logic circuit for input combination #5 is shown in Fig. 29.

4 Conclusion

This paper has presented the design of a new ternary logic family based on CMAT and magnetoresistive spin diodes. Since, these devices are primarily based on CMAT architecture which utilizes the technologies already available in MRAM production, this devices will need less supply voltage and power dissipation. Thus, being highly efficient non-volatile logic family spintronic ternary logic circuits have the potential to be the novel post Neumann architecture for high performance computing. As future work, we will perform SPICE simulation to ensure that our proposed logic circuits perform according to its design.

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